IN THE CLAIMS

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

Please cancel claims 1-23 without prejudice or disclaimer.

1-23. (Canceled)

24. (New) An arithmetic unit for adding a plurality of values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:

an input for receiving said plurality of values;

an adder for adding said plurality of values to define a result, said result being within a first range -2^{N-1} to $2^{N-1}-1$;

circuitry for performing a round on the result to define a rounded result, wherein the rounded result falls within a third range -2^{N} to $2^{N}-1+2^{(N/2)-1}$;

a detector for determining if said rounded result falls within a second range -2^{N-1} to $2^{N-1}-1$, said second range being smaller than the third range, said detector being arranged to consider only some of the bits of said rounded result; and

circuitry for modifying said rounded result in so that the result output but said arithmetic unit falls within the second range.

25. (New) A unit as claimed in claim 24, wherein three values are added together.

26. (New) A unit as claimed in claim 24, wherein said adder comprises a carry save adder stage.

27. (New) A unit as claimed in claim 26, wherein said carry save adder stage comprises a plurality of 3 to 2 carry save adders.

28. (New) A unit as claimed in claim 24, wherein said adding means comprises an adder stage for providing said result.

29. (New) A unit as claimed in claim 24, wherein said detector is arranged to take into account bits other than the considered bits.

30. (New) A unit as claimed in claim 24, wherein the second range can be expressed by N bits and bits N to N-2 of at least some of the plurality of values are considered by said detector.

31. (New) A unit as claimed in claim 24, wherein the arithmetic unit is arranged to operate in 2's complement binary arithmetic.

32. (New) A unit as claimed in claim 31, wherein a first of said plurality of values has an N bit format and falls in the range -2^{N-1} to $2^{N-1}-1$.

33. (New) A unit as claimed in claim 31, wherein the sum of a second and a third of said plurality of values falls in the range -2^{N-1} to 2^{N-1}.

34. (New) A unit as claimed in claim 24, wherein the unit is arranged such that if the detector determines that the result falls outside said second range, the modifying circuitry replaces the rounded result by a saturation value.

35. (New) A unit as claimed in claim 34, wherein the modifying circuitry is arranged to provide a first saturation value if one end of the range is exceeded and another saturation value if the other end of the range is exceeded.

36. (New) A unit as claim in claim 25, wherein at least one of the following values is calculated;

a first carry value is generated from the bits N-2 from said three values;

a second carry value is generated from the bits N-1 of said three values;

a first sum value is generated from the bits N-1 of said three values; and

a second sum is generated from the bits N of two of said values and bit N-1 of one of the values.

37. (New) A unit as claimed in claim 36, wherein said first and second carry values and said first and second sums are generated to provide first and second result values.

38. (New) A unit is claimed in claim 37, wherein the detector determines if the second range is exceeded based on said first and second results and a third carry value.

39. (New) A unit as claimed in claim 38, wherein said third carry value is determined from an addition of a sum and a carry value for bits N-2 down to 0 of said values.

40. (New) A unit as claimed in claim 24, wherein a round is performed to clear the x least significant bits of said result.

41. (New) A unit as claimed in claim 24, wherein a round is performed by adding $2^{(N/2)-1}$ to said result.

42. (New) A unit as claimed in claim 24, wherein said circuitry for modifying said result is arranged to receive information as to the sign of the total of a first and a second value and information as to one bit of a third value to determine if the result can fall out of said second range at the positive end thereof or the negative end thereof.

43. (New) A unit as claimed in claim 24, wherein said plurality of values comprise a plurality of partial products.

44. (New) A unit as claimed in claim 24, wherein said plurality of values comprise an accumulator.

45. (New) A unit as claimed in claim 24, wherein a plurality of registers are provided for storing said plurality of values.

46. (New) An arithmetic unit for adding three values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:

an input for receiving said values;

an adder for adding said values to define a result, said result being within a first range -2^{N} to $2^{N}-1$;

a detector for determining if said result falls within a second range -2^{N-1} to $2^{N-1}-1$, said second range being smaller than the first range, said detector being arranged to consider only some bits of said result; and

circuitry for modifying said result in so that the result output by said arithmetic unit falls within the second range.

47. (New) An arithmetic unit for adding three values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:

an input for receiving said values;

an adder for adding said values to define a result, said result being within a first range -2^{N} to $2^{N}-1$;

circuitry for performing a round on the result, to define a rounded result, wherein the rounded result falls within a third range -2^{N} to $2^{N}-1+2^{(N/2)-1}$;

a detector for determining if said result falls within a second range -2^{N-1} to $2^{N-1}-1$, said second range being smaller than the third range, said detector being arranged to consider only some bits of said rounded result; and

circuitry for modifying said rounded result in so that the result output by said arithmetic unit falls within the second range.

48. (New) An arithmetic unit for adding a plurality of values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:

an input for receiving said plurality of values;

an adder for adding said values to define a result, wherein said adder comprises a carry save adder stage comprising a plurality of 3 to 2 carry save adders, said result being within a first range -2^{N} to $2^{N}-1$;

a detector for determining if said result falls within a second range -2^{N-1} to $2^{N-1}-1$, said second range being smaller than the first range, said detector being arranged to consider only some bits of said result; and

circuitry for modifying said result in so that the result output by said arithmetic unit falls within the second range.

49. (New) An arithmetic unit for adding a plurality of values, each value falling within the range -2^{N-1} to $2^{N-1}-1$, to define a result, said arithmetic unit comprising:

an input for receiving said plurality of values;

an adder for adding said values to define a result, wherein said adder comprises a plurality of 3 to 2 carry save adders, said result being within a first range -2^{N} to $2^{N}-1$;

circuitry for performing a round on the result to define a rounded result, wherein the rounded result falls within a third range -2^{N} to $2^{N}-1+2^{(N/2)-1}$;

a detector for determining if said result falls within a second range -2^{N} to $2^{N-1}-1$, said second range being smaller than the third range, said detector being arranged to consider only some bits of said rounded result; and

circuitry for modifying said result in so that the result output by said arithmetic unit falls within the second range.